REMARKS

At the time the Final Official Action was mailed, the Examiner rejected claims 1-19. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Drawing Amendment

On December 23, 2004, Applicants submitted formalized drawings along with a Request for Continued Examination (RCE) and Response to Office Action. In the formalized replacement drawings submitted on December 23, 2004, a minor numbering error was injected into Fig. 1. Specifically, element numbers 16 and 18 were inadvertently reversed in the formalized replacement sheet of Fig. 1 submitted on December 23, 2004. This numbering is inconsistent with the specification and with the drawings originally filed with the application. To correct the error, Applicants hereby submit a replacement sheet for Fig. 1, attached hereto as Appendix "A," with the corrected numbering.

Rejections under 35 U.S.C. § 112, first paragraph

The Examiner rejected claims 1-19 under 35 U.S.C. § 112, first paragraph, for failing to comply with the written description requirement. Specifically, the Examiner stated:

> Claims 1-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1 and 12 recite the limitation "a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of the data associated with the request." The specification states "each transaction associated with a particular request is exchanged on a single unidirectional bus" and "each bus 30A-30K has a unique signal

> associated with it and signals are not shared between buses 30A-30K." However, the specification does not state that the signals associated with a single unidirectional bus cannot be data signals.

Applicants respectfully traverse this rejection. The initial burden of proof regarding the sufficiency of the written description falls on the Examiner. Accordingly, the Examiner must present evidence or reasons why persons skilled in the art would not recognize a description of the claimed subject matter in the applicant's disclosure. *In re Wertheim*, 541 F.2d 257, 262, 191 U.S.P.Q. 90, 96 (CCPA 1976). The Examiner is also reminded that the written description requirement does not require the claims to recite the same terminology used in the disclosure. The patentee may be his own lexicographer. *Ellipse Corp. v. Ford Motor Co.*, 171 U.S.P.Q. 513 (7th Cir. 1971), *aff'd.* 613 F.2d 775 (7th Cir. 1979), *cert. denied*, 446 U.S. 939 (1980).

Independent claims 1 and 12 each recite an internal bus structure comprising a plurality of individual buses, wherein "each of the individual buses comprises a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of the data associated with the request." The Examiner essentially asserts that the specification does not state that the internal bus structure cannot transmit data signals. However, Applicants respectfully assert that those skilled in the art would recognize a description of the claimed subject matter in the present disclosure. Specifically, those skilled in the art would appreciate that the internal data bus, when viewed in light of the specification, is not configured to transmit data signals.

As described in the present specification, a host controller generally coordinates the exchange of *requests* and *data* associated with those requests between processor buses, I/O buses and memory. Page 8, line 22 – page 9, line 1. Each *request* includes a series of ordered exchanges or transactions, each having a respective/unique signal type. Page 11, lines 9-23. As will be appreciated, a *request* for data is not the same as, nor does it include the *data* itself. To be clear, and as described throughout the present specification, "requests" include a series of ordered exchanges or transactions which are sent through the host controller via the internal bus structure, such as the internal bus structure 30 of the host controller 16. In contrast, the requested *data* is transmitted through the data controller via a *data bus*.

With specific reference to Fig. 3, the internal bus structure 30 includes a number of single unidirectional buses 30A-30K. Each of the unidirectional buses 30A-30K is configured to send one of the ordered exchanges 38A-38K having a unique signal type. For instance, the exchange sent along the individual bus 30A is a request address/command 38A. The request sent along individual bus 30B is an initial response 38B. The exchange sent along the individual bus 30C is a request snoop results 38C, and so forth. While it is clear that the particular exchanges 38A-38K may vary from system to system, it is important to note that each exchange 38A-38K has a unique signal type (e.g., request address/command, initial response, request snoop results, etc.) and that each of those exchanges 38A-38K having a unique signal type is sent through the internal bus structure on a respective one of the single unidirectional buses 30A-30K. It is abundantly clear from Fig. 3 and the associated detailed description, as well as the entire specification, that the disclosed and recited internal bus structure is configured to send the ordered exchanges or transactions associated with a particular request.

In contrast, the *data* associated with the request is not sent via the internal bus structure 30. Those skilled in the art would appreciate that the data associated with a particular request is not sent along the internal bus structure, but rather is sent on a data bus which is not illustrated in the present figures. Those skilled in the art would appreciate that the data is exchanged on a data bus through the data controller 18 under the direction of the host controller 16. The specific configuration of the data bus inside the data controller is not within the intended scope of the present claims and is therefore not illustrated. Indeed, the omission of the data bus in the figures makes clear that embodiments of the present invention are directed to the internal bus structure which is configured to transmit the ordered exchanges associated with a particular request and not the data associated with that request.

Applicants respectfully submit that in light of the present specification, those skilled in the art will fully appreciate the intended scope of the claims and will understand that the internal bus structure recited in the present claims is not employed to exchange data signals. Thus, Applicants were clearly in possession of the claimed invention at the time of filing, and those skilled in the art would fully recognize the description of the claimed subject matter in the specification. Because Applicants respectfully submit that those skilled in the art would recognize the description of the claimed subject matter in the present specification, Applicants respectfully submit that the written description requirement is fulfilled. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection under 35 U.S.C. § 112, first paragraph.

Rejections under 35 U.S.C. § 112, second paragraph

The Examiner rejected claims 1-19 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Examiner stated:

> In reference to claims 1 and 12, it is unclear how data is transmitted between the processor, the memory, and the cache memory if each of the individual buses of the internal bus controller is configured to transmit only one signal type associated with the request and not data associated with the request.
>
> In reference to claims 1, it is unclear if the enchange of a request and data associated with the request occur between the processor, the main memory, and the cache memory all at once or if it only occurs between two of them at once.

Applicants respectfully traverse this rejection. In ruling on a claim of patent indefiniteness, a court must determine whether those skilled in the art would understand what is claimed when the claim is read in light of the specification. *Personalized Media Communications, Inc. v. Int'l Trade Comm'n*, 161 F.3d 696, 705, 48 U.S.P.Q.2d 1880 (Fed. Cir. 1998); *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 U.S.P.Q.2d 1081 (Fed. Cir. 1986). A claim in not indefinite merely because it poses a difficult issue of claim construction; if the claim is subject to construction, i.e., it is not insolubly ambiguous, it is not invalid for indefiniteness. *Honeywell Int'l, Inc. v. Int'l Trade Comm'n*, 341 F.3d 1332, 1338-39, 68 U.S.P.Q.2d 1023 (Fed. Cir. 2003). That is, if the meaning of the claim is discernible, even though the task may be formidable and the conclusion may be one over which reasonable persons disagree, a claim is sufficiently clear to avoid invalidity on indefiniteness grounds. *Exxon Research & Eng'g Co. v. United States*, 265 F.3d 1371, 1375, 60 U.S.P.Q.2d 1272 (Fed. Cir. 2001).

With regard to the Examiner's first point, the Examiner submits that "it is unclear how data is transmitted between the processor, the memory and the cache memory if each of the individual buses of the internal bus structure is configured to transmit only one signal type associated with the request and not data associated with the request." However, as set forth above in the discussion under the rejections under 35 U.S.C. § 112, first paragraph, Applicants respectfully assert that those skilled in the art would understand that the internal bus structure recited in the present claims is *not* a data bus. The data bus is not illustrated in the present figures, nor is it recited in the present claims. Applicants further assert that those skilled in the art would fully appreciate that the data associated with the recited "request" is sent on a data bus by any one of a number of conventional means. Again, the present claims are directed, in part, to the internal bus structure for transmitting the series or ordered exchanges or transactions that are associated with a request and *not* with the data bus. For these reasons, Applicants respectfully submit that claims 1 and 12 are not indefinite when read in light of the specification.

With regard to the Examiner's second point, the Examiner asserts that "it is unclear if the exchange of a request and data associated with the request occur between the processor, the main memory, and the cache memory all at once or if it only occurs between two of them at once." Applicants respectfully submit that the Examiner's statement is not relevant to the scope of claim 1. That is, Applicants do not claim a relationship or concurrency in transmitting the requests and the data associated with the requests. There is no recitation in independent claim 1 of how data is transmitted between the processor, the memory, and the cache memory, because such data transmission is not required to define the present invention, and thus, is beyond the scope of the recited subject matter. Applicants submit that any

discussions in the specification regarding concurrency or transmission order are described with regard to the ordered exchanges or transactions that are part of each request and not with the data associated with each request.

For at least the reasons set forth above, Applicants respectfully submit that claims 1-19 are definite in view of the present specification. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejections under 35 U.S.C. § 112, second paragraph.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1-6 and 12-16 under 35 U.S.C. § 103 (a) as being unpatentable over U.S. Patent No. 5,802,269 to Poisner et al. (herein referred to as "the Poisner reference") and U.S. Publication No. 2002/0120878 to Lapidus (herein referred to as "the Lapidus reference").

Applicants respectfully traverse this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

Independent claim 1 recites a system comprising a host controller "configured to coordinate the exchange of a request and data associated with the request between the processor, the main memory and the cache memory." Claim 1 further recites an internal bus structure "configured to transmit the request comprising a plurality of ordered transactions each having a unique signal type, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of the data associated with the request." Similarly, claim 12 recites an internal bus structure, "configured to transmit a request comprising a plurality of ordered transactions each having a unique signal type, and each of the individual buses comprising a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of data associated with the request." Applicants respectfully submit that neither of the references disclose the recited elements.

The Examiner admitted that "Poisner does not teach that each of the individual buses comprises a unidirectional bus configured to transmit only one signal type." *See* Official Action mailed March 16, 2005, page 3. Indeed, the Poisner reference simply discloses a system that includes a bridge 33 coupled to a cache 39, a central processing unit (CPU) 31, and a main memory 35, and operates in a DDMA environment. *See id.* at Fig. 1; col. 3, lines 59-67. Poisner is completely silent with regard to the *internal bus structure*, and thus does not disclose a unidirectional bus configured to transmit *only one signal type of a plurality of signal types that are utilized to process a particular request operation* in a host controller. Thus, as recognized by the Examiner, the Poisner reference does not teach or disclose the claimed subject matter.

To cure these deficiencies in the Poisner reference, the Examiner cited the Lapidus reference. Specifically, the Examiner stated, "Lapidus teaches a bus structure having a plurality of unidirectional request signal lines that are separate from the data lines (See Page 3 Paragraph 33). Lapidus further teaches that each of the unidirectional request signal lines transmits only one unique signal type, namely REQUEST IN or REQUEST OUT (See Page 3 Paragraphs 38-41). Thus, the Examiner appears to have correlated "REQUEST IN" and "REQUEST OUT" as the recited "signal types," and asserts that the REQUEST IN bus and the REQUEST OUT bus are equivalent to the recited unidirectional buses. Applicants respectfully traverse this assertion.

As described in the present specification, and discussed in detail above, a host controller generally coordinates the exchange of requests *and* data associated with those requests between processor buses, I/O buses and memory. Page 8, line 22 – page 9, line 1. *Each request* includes a series of ordered exchanges or transactions, each having a respective/unique signal type. Page 11, lines 9-23. Advantageously, by executing each transaction associated with a request on a separate, individual bus, routing congestion is minimized. Page 11, line 23 – page 12, line 1. In light of the present specification, it is clear that the disclosed internal bus structure is configured to transmit *request* transactions, not *data* associated with the request. Further, the internal bus structure is provided to transmit a plurality of ordered transactions associated with *each* request.

Independent claims 1 and 12 each recite an internal bus structure "configured to transmit a request comprising a plurality of ordered transactions each having a unique signal

type, and each of the individual buses comprising a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of data associated with the request." The Examiner correlated the REQUEST IN bus and the REQUEST OUT bus with the recited unidirectional buses configured to transmit only one unique signal type. However, while the REQUEST IN and REQUEST OUT buses of Lapidus are described as unidirectional buses, the request buses of Lapidus are not configured to transmit only one unique signal type. Each bus is used to transmit any and all request signals to or from the associated bus device 210. The Lapidus reference simply teaches that requests going to (IN) a bus device 210 are sent on one unidirectional bus (i.e., REQUEST IN) and requests going from (OUT) a bus device 210 are sent on a different unidirectional bus (i.e., REQUEST OUT). Each REQUEST IN and REQUEST OUT bus is configured to transmit a number of signal types, according to Lapidus. "The request bus contains address lines, byte enable lines (32-bit or 64-bit data reads), cycle type lines, and routing information for transactions." Lapidus, Paragraph [0033]. The Lapidus reference does not disclose or suggest anything about the specific internal configuration of the request buses (REQUEST IN and REQUEST OUT), the types of signals transmitted and how those signal types are transmitted, much less that the request bus comprises "a plurality of individual buses...configured to transmit a request comprising a plurality of ordered transactions each having a unique signal type, and each of the individual buses comprising a unidirectional bus configured to transmit only one signal type associated with the request," as recited in claims 1 and 12. For this reason, it is clear that the Lapidus reference does not cure the deficiencies of the Poisner reference with regard to the independent claims.

Further, if the Examiner is attempting to correlate incoming requests as one unique signal type, and outgoing requests as another unique signal type, the Examiner's rejection also fails to render the recited subject matter obvious. As discussed above, the present claims recite that each request comprises a plurality of ordered transactions each having a unique signal type. That is, as single request comprises a plurality of ordered transactions. For the Examiner to assert that the transactions sent on the REQUEST IN bus have one unique signal type and the transactions sent on the REQUEST OUT bus have another unique signal type, each of these transactions would have to correspond to the same request. However, as discussed above, requests to bus device 210 are sent on the REQUEST IN bus, while requests being from the bus device 210 are sent on the REQUEST OUT bus. Thus, the requests sent on the REQUEST IN bus are not even the same requests as are sent on the REQUEST OUT bus. Thus, even under this interpretation, it is clear that the cited combination fails to teach our suggest the subject matter recited in independent claims 1 and 12.

Because the cited references do not disclose each of the features recited in independent claims 1 and 12, the references cannot render the claimed subject matter obvious. Therefore, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 1-6 and 12-16.

Additional Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 7, 8, 17 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Poisner in view of Lapidus and Hanaoka et al. (U.S. Patent No. 6,584,103). The Examiner rejected claims 9 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Poisner in view of Lapidus, Hanaoka, and Ketseoglou et al. (U.S. Patent No. 6,130,886). The

Examiner rejected claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Poisner in view of Lapidus and Miyao et al. (U.S. Patent No. 5,901,281). Finally, the Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Poisner in view of Lapidus and Deshpande et al. (U.S. Patent No. 6,587,930).

Applicants respectfully assert that the cited references, alone or in combination, fail to render the claimed subject matter obvious, because none of the additional references cure the deficiencies of the Poisner and Lapidus references discussed above with regard to claims 1 and 12. Each of the claims 7-11 and 17-19 depend from independent claim 1 or 12 and are allowable based on their dependency on allowable base claims. Because the cited references fail to disclose all of the claimed subject matter, even if otherwise they could be combined, the references cannot be combined to establish a *prima facie* case of obviousness. Therefore, Applicants respectfully request withdrawal of the rejections and allowance of claims 7-11 and 17-19.

Conclusion

In view of the remarks set forth above, Applicants respectfully request reconsideration of the Examiner's rejections and allowance of claims 1-19. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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